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PTO-1449 (Modified) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. 211.004-US	SERIAL NUMBER 10/E40,009
	APPLICANT(S) Ferrant et al.	
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U.S. PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION TERMS

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

4)	"A Capacitorless Double-Gate DRAM Cell", Kuo et al., IEEE Electron Device Letters, Vol. 23, No. 6, June 2002, pp.345-347
	"A Capacitorless Double-Gate DRAM Cell for High Density Applications", Kuo et al., IEEE IEDM, 2002, pp.843-846
	"The Multi-Stable Behaviour of SOI-NMOS Transistors at Low Temperatures", Tack et al., Proc. 1988 SOS/SOI Technology Workshop (Sea Palms Resort, St. Simons Island, GA, Oct. 1988), p.78
	"The Multistable Charge-Controlled Memory Effect in SOI MOS Transistors at Low Temperatures", Tack et al., IEEE Transactions on Electron Devices, Vol. 37, No. 5, May 1990, pp.1373-1382
	"Mechanisms of Charge Modulation in the Floating Body of Triple-Well nMOSFET Capacitor-less DRAMs", Villaret et al., Proceedings of the INFOS 2003, Insulating Films on Semiconductors, 13th Bi-annual Conference, June 18-20, 2003, Barcelona (Spain), (4 pages)
	"A Memory Using One-Transistor Gain Cell on SOI (FBC) with Performance Suitable for Embedded DRAM's", Ohsawa et al., 2003 Symposium on VLSI Circuits Digest of Technical Papers, June 2003 (4 pages)
	"FBC (Floating Body Cell) for Embedded DRAM on SOI, Inoh et al., 2003 Symposium on VLSI Circuits Digest of Technical Papers, June 2003 (2 pages)
4)	"Toshiba's DRAM Cell Piggybacks on SOI Wafer", Y. Hara, EE Times, June 2003

EXAMINER SON DINH	DATE CONSIDERED 12/9/04
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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SI B CLASS	TRANSLATION YES/NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

51	"Memory Design Using a One-Transistor Gain Cell on SOI", Ohsawa et al., IEEE Journal of Solid-State Circuits, Vol. 37, No. 11, November 2002, pp.1510-1522
	"Opposite Side Floating Gate SOI FLASH Memory Cell", Lin et al., IEEE, March 2000, pp.12-15
	"Advanced TFT SRAM Cell Technology Using a Phase-Shift Lithography", Yamanaka et al., IEEE Transactions on Electron Devices, Vol. 42, No. 7, July 1995, pp.1305-1313
	"Soft-Error Characteristics in Bipolar Memory Cells with Small Critical Charge", Idei et al., IEEE Transactions on Electron Devices, Vol. 38, No. 11, November 1991, pp.2465-2471
	"An SOI 4 Transistors Self-Refresh Ultra-Low-Voltage Memory Cell", Thomas et al. IEEE, March 2003, pp.401-404
	"Design of a SOI Memory Cell", Stanojevic et al., IEEE Proc. 21 st International Conference on Microelectronics (MIEL '97), Vol. 1, NIS, Yugoslavia, 14-17 September 1997, pp.297-300
	"Effects of Floating Body on Double Polysilicon Partially Depleted SOI Nonvolatile Memory Cell", Chan et al., IEEE Electron Device Letters, Vol. 24, No. 2, February 2003, pp.75-77
	"MOSFET Design Simplifies DRAM", P. Fazan, EE Times, May 14, 2002 (3 pages)
	"One of Application of SOI Memory Cell - Memory Array", Lončar et al., IEEE Proc. 22 nd International Conference on Microelectronics (MIEL 2000), Vol. 2, NIŠ, Serbia, 14-17 May 2000, pp.455-458
	"A SOI Current Memory for Analog Signal Processing at High Temperature", Portmann et al., 1999 IEEE International SOI Conference, Oct. 1999, pp.18-19
51	"Chip Level Reliability on SOI Embedded Memory", Kim et al., Proceedings 1998 IEEE International SOI Conference, Oct. 1998, pp.135-139

EXAMINER SON DINH	DATE CONSIDERED 12/9/04
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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION REQUIRED

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

51	"Analysis of Floating-Body-Induced Leakage Current in 0.15µm SOI DRAM", Terauchi et al., Proceedings 1998 IEEE International SOI Conference, Oct. 1998, pp.138-139
	"Programming and Erase with Floating-Body for High Density Low Voltage Flash EEPROM Fabricated on SOI Wafers", Chi et al., Proceedings 1995 IEEE International SOI Conference, Oct. 1995, pp.129-130
	"Measurement of Transient Effects in SOI DRAM/GRAM Access Transistors", A. Wal, IEEE Electron Device Letters, Vol. 17, No. 5, May 1998, pp.193-195
	"In-Depth Analysis of Opposite Channel Based Charge Injection in SOI MOSFETs and Related Defect Creation and Annihilation", Sinha et al., Elsevier Science, Microelectronic Engineering 28, 1995, pp.383-388
	"Dynamic Effects in SOI MOSFETs", Giffard et al., IEEE, 1991, pp.180-181
	"A Simple 1-Transistor Capacitor-Less Memory Cell for High Performance Embedded DRAMs", Fazan et al., IEEE 2002 Custom Integrated Circuits Conference, June 2002, pp.99-102
	"A Novel Pattern Transfer Process for Bonded SOI Giga-bit DRAMs", Lee et al., Proceedings 1996 IEEE International SOI Conference, Oct. 1998, pp.114-115
	"An Experimental 2-bit/Cell Storage DRAM for Macrocell or Memory-on-Logic Application", Furuyama et al., IEEE Journal of Solid-State Circuits, Vol. 24, No. 2, April 1989, pp.388-393
	"High-Performance Embedded SOI DRAM Architecture for the Low-Power Supply", Yamauchi et al., IEEE Journal of Solid-State Circuits, Vol. 35, No. 8, August 2000, pp.1169-1178
	"An SOI-DRAM with Wide Operating Voltage Range by CMOS/SIMOX Technology", Suma et al., 1994 IEEE International Solid-State Circuits Conference, pp.138-139
51	"A Capacitorless DRAM Cell on SOI Substrate", Wann et al., IEEE IEDM, 1993, pp.635-638

EXAMINER SON DINH	DATE CONSIDERED 12/9/04
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

41)	"The Multistable Charge Controlled Memory Effect in SOI Transistors at Low Temperatures". Tack et al., IEEE Workshop on Low Temperature Electronics, 7-8 Aug. 1989, University of Vermont, Burlington, pp.137-141
	"High-Endurance Ultra-Thin Tunnel Oxide in MONOS Device Structure for Dynamic Memory Application", Wann et al., IEEE Electron Device Letters, Vol. 16, No. 11, November 1995, pp.491-493
	"Hot-Carrier Effects in Thin-Film Fully Depleted SOI MOSFETs", Ma et al., IEEE Electron Device Letters, Vol. 15, No. 6, June 1994, pp.218-220
	"Design Analysis of Thin-Body Silicide Source/Drain Devices", 2001 IEEE International SOI Conference, October 2001, pp.21-22
	"SOI MOSFET on Low Cost SPI-MOX Substrate", Iyer et al., IEEE IEDM, September 1998, pp.1001-1004
	"Simulation of Floating Body Effect in SOI Circuits Using BSIM3SOI", Tu et al., Proceedings of Technical Papers (IEEE Cat No. 97 TH 8303), pp.339-342
	"High-Field Transport of Inversion-Layer Electrons and Holes Including Velocity Overshoot", Assaderaghi et al., IEEE Transactions on Electron Devices, Vol. 44, No. 4, April 1997, pp.664-671
	"Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage VLSI", Assaderaghi et al., IEEE Transactions on Electron Devices, Vol. 44, No. 3, March 1997, pp.414-422
	"Hot-Carrier-Induced Degradation in Ultra-Thin-Film Fully-Depleted SOI MOSFETs", Yu et al., Solid-State Electronics, Vol. 39, No. 12, 1996, pp.1791-1794
41)	"Hot-Carrier Effect in Ultra-Thin-Film (UTF) Fully-Depleted SOI MOSFETs", Yu et al., 54 th Annual Device Research Conference Digest (Cat. No. 96 TH 8193), pp.22-23

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

4D	"SOI MOSFET Design for All-Dimensional Scaling with Short Channel, Narrow Width and Ultra-thin Films", Chan et al., IEEE IEDM, 1995, pp.631-634
	"A Novel Silicon-On-Insulator (SOI) MOSFET for Ultra Low Voltage Operation", Assaderaghi et al., 1994 IEEE Symposium on Low Power Electronics, pp.68-69
	"Interface Characterization of Fully-Depleted SOI MOSFET by a Subthreshold IV Method", Yu et al., Proceedings 1994 IEEE International SOI Conference, Oct. 1994, pp.63-64
	"A Capacitorless Double-Gate DRAM Cell Design for High Density Applications", Kuo et al., IEEE IEDM, Feb. 2002, pp.843-846
	"A Dynamic Threshold Voltage MOSFET (DTMOS) for Ultra-Low Voltage Operation", Assaderaghi et al., IEEE Electron Device Letters, Vol. 15, No. 12, December 1994, pp.510-512
	"Dynamic Threshold-Voltage MOSFET (DTMOS) for Ultra-Low Voltage Operation", Assaderaghi et al., 1994 IEEE, IEDM 94, pp.809-812
	"A Capacitorless DRAM Cell on SOI Substrate", Wann et al., IEEE IEDM 1993, pp.835-838
	"Studying the Impact of Gate Tunneling on Dynamic Behaviors of Partially-Depleted SOI CMOS Using BSIMPD", Su et al., IEEE Proceedings of the International Symposium on Quality Electronic Design (ISQED '02), April 2002 (5 pages)
	"Characterization of Front and Back Si-SiO ₂ Interfaces in Thick- and Thin-Film Silicon-on-Insulator MOS Structures by the Charge-Pumping Technique", Wouters et al., IEEE Transactions on Electron Devices, Vol. 36, No. 9, September 1989, pp.1746-1750
4D	"An Analytical Model for the Misis Structure in SOI MOS Devices", Tack et al., Solid State Electronics Vol. 33, No. 3, 1990, pp.357-364

EXAMINER SON DINH	DATE CONSIDERED 12/9/04
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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

SD	"A Long Data Retention SOI DRAM with the Body Refresh Function", Tomishima et al., IEICE Trans. Electron., Vol. E80-C, No. 7, July 1997, pp.899-904
	"A Simple 1-Transistor Capacitor-Less Memory Cell for High Performance Embedded DRAMs", Fazan et al., IEEE 2002 Custom Integrated Circuits Conference, June 2002, pp.99-102
	"High-Endurance Ultra-Thin Tunnel Oxide in MONOS Device Structure for Dynamic Memory Application", Wann et al., IEEE Electron Device Letters, Vol. 16, No. 11, November 1995, pp.491-493
	"Capacitor-Less 1-Transistor DRAM", Fazan et al., 2002 IEEE International SOI Conference, Oct 2002, pp.10-13
	"SOI (Silicon-on-Insulator) for High Speed Ultra Large Scale Integration", C. Hu, Jpn. J. Appl. Phys. Vol. 33 (1994) pp.385-369, Part 1, No. 1B, January 1994
	"Source-Bias Dependent Charge Accumulation in P+ -Poly Gate SOI Dynamic Random Access Memory Cell Transistors", Sim et al., Jpn. J. Appl. Phys. Vol. 37 (1998) pp.1260-1283, Part 1, No. 3B, March 1998
SD	"Suppression of Parasitic Bipolar Action in Ultra-Thin-Film Fully-Depleted CMOS/SIMOX Devices by Ar-Ion Implantation into Source/Drain Regions", Ohno et al., IEEE Transactions on Electron Devices, Vol. 45, No. 5, May 1998, pp.1071-1076

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OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

SD	"Fully Isolated Lateral Bipolar-MOS Transistors Fabricated in Zone-Melting-Recrystallized Si Films on SiO ₂ ", Tsaur et al., IEEE Electron Device Letters, Vol. EDL-4, No. 8, August 1983, pp.269-271
	"Silicon-On-Insulator Bipolar Transistors", Rodder et al., IEEE Electron Device Letters, Vol. EDL-4, No. 8, June 1983, pp.193-195
	"Characteristics and Three-Dimensional Integration of MOSFET's in Small-Grain LPCVD Polycrystalline Silicon", Malhi et al., IEEE Transactions on Electron Devices, Vol. ED-32, No. 2, February 1985, pp.258-281
	"Triple-Well nMOSFET Evaluated as a Capacitor-Less DRAM Cell for Nanoscale Low-Cost & High Density Applications", Villaret et al., Handout at Proceedings of 2003 Silicon Nanoelectronics Workshop, June 8-9, 2003, Kyoto, Japan (2 pages)
	"Mechanisms of Charge Modulation in the Floating Body of Triple-Well NMOSFET (Capacitor-less DRAMs)", Villaret et al., Handout at Proceedings of INFOS 2003, June 18-20, 2003, Barcelona, Spain (2 pages)
	"Embedded DRAM Process Technology", M. Yamawaki, Proceedings of the Symposium on Semiconductors and Integrated Circuits Technology, 1998, Vol. 55, pp.38-43
	"3-Dimensional Simulation of Turn-off Current in Partially Depleted SOI MOSFETs", Ikeda et al., IEIC Technical Report, Institute of Electronics, Information and Communication Engineers, 1998, Vol. 97, No. 557 (SDM97 186-198), pp.27-34
SD	"DRAM Design Using the Taper-Isolated Dynamic RAM Cell, Leiss et al.", IEEE Transactions on Electron Devices, Vol. ED-29, No. 4, April 1982, pp.707-714

EXAMINER SON DINH	DATE CONSIDERED 12/9/04
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CA	FR 2 197 484	3/1974	French			
	EP 1 180 799	2/2002	European			
	EP 0 030 856	6/1981	European			
	GB 1 414 228	11/1975	Great Britain			
	EP 0 694 977	1/1986	European			
	EP 1 237 193	9/2002	European			
	EP 0 878 804	11/1988	European			
	EP 0 801 427	10/1997	European			
	EP 0 513 923	11/1992	European			
	EP 0 731 972	11/2001	European			
	EP 0 362 961	2/1994	European			
	EP 1 288 955	3/2003	European			
CA	EP 1 280 205	1/2003	European			

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FOREIGN PATENT DOCUMENTS

EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATOR YEAR
CD	EP 1 253 634 A2	10/2002	European			
	EP 1 241 708 A2	9/2002	European			
	EP 1 209 747 A2	5/2002	European			
	EP 1 204 147 A1	5/2002	European			
	EP 1 204 146 A1	5/2002	European			
	EP 1 179 850 A2	2/2002	European			
	EP 1 182 744 A1	12/2001	European			
	EP 1 182 663 A2	12/2001	European			
	EP 1 073 121 A2	1/2001	European			
	EP 0 993 037 A2	4/2000	European			
	EP 0 980 101 A2	2/2000	European			
	EP 0 971 360 A1	1/2000	European			
	EP 0 951 072 A1	10/1999	European			
CD	EP 0 933 820 A1	8/1999	European			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
41	EP 0 924 766 A2	6/1999	European			
	EP 0 920 059 A2	6/1999	European			
	EP 0 869 511 A2	10/1998	European			
	EP 0 860 878 A2	8/1998	European			
	EP 0 868 189 A2	8/1998	European			
	EP 0 844 671 B1	11/2002	European			
	EP 0 836 194 B1	5/2000	Européan			
	EP 0 788 165 A2	8/1997	European			
	EP 0 744 772 B1	8/2002	European			
	EP 0 739 097 A2	10/1996	European			
	EP 0 727 822 B1	8/1999	European			
	EP 0 727 820 A1	8/1996	European			
41	EP 0 726 801 B1	9/2001	European			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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CD	EP 0 725 402 B1	9/2002	European			
	EP 0 689 252 B1	8/2000	European			
	EP 0 682 370 B1	9/2000	European			
	EP 0 642 173 B1	7/1999	European			
	EP 0 608 758 B1	9/2000	European			
	EP 0 601 590 B1	4/2000	European			
	EP 0 599 506 A1	6/1994	European			
	EP 0 599 388 B1	8/2000	European			
	EP 0 579 566 A2	1/1994	European			
	EP 0 564 204 A2	10/1993	European			
	EP 0 537 677 B1	8/1998	European			
	EP 0 510 607 B1	2/1998	European			
CD	EP 0 465 961 B1	8/1995	European			

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

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EXAMINER INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION VERSION
SN	EP 0 366 882 B1	5/1995	European			
	EP 0 359 551 B1	12/1994	European			
	EP 0 354 348 A2	2/1990	European			
	EP 0 350 057 B1	1/1990	European			
	EP 0 333 426 B1	7/1996	European			
	EP 0 300 157 B1	5/1993	European			
	EP 0 253 631 B1	4/1992	European			
	EP 0 245 515 B1	4/1997	European			
	EP 0 207 619 B1	8/1991	European			
	EP 0 202 515 B1	3/1991	European			
	EP 0 175 378 B1	11/1991	European			
	EP 1 191 596 A2	3/2002	European			
SN	EP 1 233 454 A2	8/2002	European			

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